REMARKS

The Pending Claims and Amendments

Claims 38-67 and 69-75 were pending prior to this response. By this amendment, claim 69 been cancelled. New claims 76-94 have been submitted for entry. Therefore, the currently pending claims are 38-67 and 70-94.

Independent claims 38, 57, and 58 have been amended. Also, dependent claims 41 and 73-75 have been amended to correct typographical errors. Support for the amendments to the independent claims is found at paragraph [0029] and in the figures, particularly Figure 3B, Figure 4B, and Figure 5D.

Support for new claims 76, 80, and 86 is found at is found at paragraph [0037]. Support for claims 77, 81, and 87 is found at paragraph [0054]. Support for new claim 78 is found at paragraph [0060]. Support for new claims 79, 85 and 91 is found in Figure 6A and the associated discussion in the specification. Finally, support for new claims 82-84 and 88-88 is found at paragraph [0045]. Support for new claims 92-94 is found in paragraph [0053] and in Fig. 6A.

Note that all references to "fluorine" in the specification and claims have been changed to "fluorene." It will be understood by those of skill in the art that use of "fluorine" to describe semiconductor polymers is a typographical error. The only plausible related term for compounds belonging to the corresponding classes of compounds recited in the specification is "fluorene," which has a similar pronunciation to "fluorine." If the Examiner has any questions or concerns about this correction, numerous references can be provided to show that fluorene compounds belong to the class of semiconductors recited in the instant specification.

The application contains three independent claims, claims 38, 57, and 58, each reciting a method of forming a display by forming *pixel control circuits* on a substrate. Claim 38 specifies that forming the pixel control circuits includes "depositing a semiconductor from a solution." Claim 57 specifies that forming the pixel control circuits includes "patterning an organic semiconductor." Claim 58 specifies that forming the pixel control circuits includes forming at least one electrode that includes "an organic conductor."

In the Office Action, all claims were rejected. Claims 38-41, 44-45, 49, 51-54, 57, 70, and 72-73 were rejected as anticipated by US Patent Publication No. 2002/0179901 by Arai et al. Claims 42, 43, 46-48, 50, 55, 56, 67, 69, 71, 74, and 75 were rejected as obvious over a combination of Arai et al. and various other references. Claims 58-66 were rejected as

anticipated by US Patent No. 6,177,921 to Comiskey et al. Applicant respectfully traverses all rejections in view of the amendments and remarks presented herein.

Interview

Applicant appreciates the courtesy of the telephonic interview extended to the undersigned representative by the Examiner on December 13, 2005. During that interview, the pending claims were discussed along with the Arai et al. and Fujita et al. (USP 5,042,917) references. The undersigned agreed to limit independent claims 38, 57, and 58 to methods of forming pixel control circuits having two terminal switching devices. The undersigned explained why Arai et al. and Fujita et al. references were directed to fundamentally different structures (transistors versus diodes) and why the differences in these structures led to fundamentally different fabrication considerations. No agreement was reached.

Rejections based on Arai et al. (and Fujita et al.)

By this response, each independent claim was amended to specify that the pixel control circuit comprises "at least one two-terminal switching device." Further, the amended claims recite fabrication sequences for electrode and semiconductor elements of the two-terminal switching devices. For example, claim 38 recites the following sequence:

> forming a first electrode of the switching device;
> depositing a semiconductor from a solution over at least a portion of the first electrode; and
> forming a second electrode over at least a portion of the semiconductor and overlying at least a portion of the first electrode.

Regarding these claims, Applicant wishes to make two initial points. First, the claims pertain to "pixel control circuits," which should be distinguished from "front plane" pixel components such as LED and LCD display elements. Second, the manufacturing operations recited in the independent claims specify the relative location of a semiconductor with respect to two electrodes. As will be explained more fully below, this arrangement presents design and engineering considerations that are incompatible with conventional three-terminal control circuits such as transistors.

Applicant notes that previously presented dependent claim 69 (now canceled) recites pixel control circuits that are "two-terminal circuits." This claim was rejected under section 103 over a combination of the Arai et al. and Fujita et al. references. Therefore, this response will focus on these references.

Applicant acknowledges that both Arai et al. and Fujita et al. describe processes for forming pixel control circuitry in displays. However, the relevant similarities end there. Arai describes a process of forming a pixel control circuit that includes a thin film transistor (TFT). Its fabrication and structure is illustrated most clearly in Figures 2A-2E and the associated discussion. Fujita describes a process of forming a pixel control circuit including a thin film diode (TFD) as shown most clearly in Figure 2a. As can be appreciated by those of skill in the art, the pixel control circuitry manufactured in these two references employs fundamentally different structures, current-voltage (I-V) characteristics, and manufacturing considerations.

Further, while the Fujita et al. diodes have a structure similar to that recited in the claims, nothing in the Fujita et al. reference suggests a method employing (1) depositing a semiconductor from a solution, (2) patterning an organic semiconductor, or (3) using an organic conductor (independent claims 38, 57, and 58 respectively). Neither Arai et al. nor any other cited reference provides the necessary motivation to make any of these changes to Fujita et al.

Arai et al. describe fabricating an organic semiconductor in a TFT by (1) depositing the semiconductor in a defined opening within a permanent structure and then (2) performing CMP to remove excess semiconductor. Fujita et al. describe an entirely inorganic diode structure, one fabricated by conventional inorganic physical vapor deposition techniques including conventional patterning and masking procedures. The processes of forming these two devices are not compatible or combinable.

At a fundamental level, the different properties and applications for transistor and diode switching devices are well know to those of skill in the art. One notable difference that impacts both manufacturing and structure is in the "critical dimension" of a TFD such as that described in Fujita et al. and a TFT such as that described in Arai et al. The critical dimension is defined by the current path between a source electrode and a drain electrode (or between an anode and a cathode). Small changes in this separation distance can greatly impact the switching characteristics of the device. In a TFT, the distance that requires critical control in order to provide desired I-V switching characteristics is the channel region between the source and drain. This is a horizontal dimension as shown in Figure 2E of Arai et al. It is controlled using a photolithographic mask in Arai et al. In a TFD, the critical distance is the separation between the two metal electrodes in, for example, an MSM or MIM diode. This is a vertical dimension as shown in Figure 2(a) of Fujita (semiconductor layer 5). It is controlled by carefully monitoring the deposition thickness of the semiconductor layer.

In a TFD, if the thickness and quality of the deposited semiconductor (or insulator in a MIM structure) is not carefully controlled, significant leakage occurs, resulting in a pronounced deviation from the required I-V switching characteristics.

To further explain this point, Arai's TFT employs an organic semiconductor film 106 deposited on an insulating film having an opening that effectively defines a permanent mold for the semiconductor in the device. (It is essentially a Damascene structure.) As shown in Figures 2C through 2E, the Arai TFT is completed by removing an upper portion of the semiconductor layer to the point of exposing the upper surface of the insulating layer and then patterning a conductive film on top of the semiconductor layer to form source and drain electrodes 108 and 109. As indicated, the critical dimension of Arai's TFT is the separation between these source and drain electrodes. The thickness of Arai's semiconductor layer is not critical to realizing a desired I-V switching characteristic.

Other features of the semiconductor deposition processes of Arai and Fujita illustrate their incompatibility. For example, while Arai deposits the semiconductor layer in a pre-formed well (defined in insulating film 105 of Figure 2B), Fujita forms the semiconductor layer (reference number 5) using a temporary mask. See e.g., Column 4, lines 50-54 of Fujita. Further, Arai uses CMP to partially remove material from the top of the deposited semiconductor film 106. If CMP were to be applied to semiconductor layer 5 in Fujita's device, it would require extreme control; the end point could not be easily detected. Generally performing CMP on a semiconductor layer in a two-terminal device such as a TFD of Fujita would be highly unadvisable. Obviously, no such material removal process is proposed by Fujita. The semiconductor layer is used without removing any material from upper regions.

Finally, Fujita's semiconductor layer 5 is formed by evaporation or sputtering of an amorphous inorganic material. The patent does not suggest any reason why one might want to substitute this deposition technique or the inorganic material it deposits. For at least the above reasons, one of skill in the art would not be led to substitute Fujita's deposition process or semiconductor material for a process or material employed in Arai.

The Examiner suggests that motivation to combine Arai and Fujita may be found based on "easy manufacturing." It is respectfully submitted that this in itself is insufficient motivation to combine the two references. When considering the respective device structures and manufacturing techniques (characteristics relevant to the pending claims), there is insufficient motivation to combine to the two references. As explained, the references describe fundamentally different processes for producing fundamentally different structures. It is therefore respectfully submitted that all pending claims are patentable over Arai et al. and Fujita et al., whether considered alone or in combination.

Rejections based on Cominskey et al.

Independent claim 58 was rejected as anticipated by US Patent No. 6,177,921 issued to Comiskey. The sections of the patent cited by the Examiner to reject the broad claims describes a passive matrix device. It does not provide not individual control circuitry for each pixel. The intersections of the row and column lines do not comprise two-terminal switching devices. (See e.g., the discussion at column 14, line 30 to column 15, line 54, and Figures 14 and 15 of the Comiskey patent). In embodiments employing organic conductors, the column and row access lines straddle an electrophoretic medium. Thus, the pertinent disclosure does not describe pixel control circuitry, and certainly not "at least one two-terminal switching device" as part of the pixel control circuitry.

Comiskey does describe active matrix pixel control devices at column 16, line 42 to column 18, line 3. However, these devices are made from silicon-based materials formed by standard IC fabrication procedures. The materials and fabrication techniques for forming these are not relevant to the claimed invention.

Other Art Rejections

In rejecting various dependent claims, various other references were cited in combination with the Arai et al. reference to support section 103 rejections. These other references are Li et al., U.S. Patent No. 6,372,154; Wudl et al., U.S. Patent No. 5,189,136; Imazeki et al., U.S. Patent No. 5,357,357; Bao et al., U.S. Patent No. 6,891,237; Lamotte et al., U.S. Publication No. 2003/0170454; Yamada et al., U.S. Publication No. 2002/0027636; Ohya et al., U.S. Publication No. 2002/0127821; and Bird et al., U.S. Patent No. 5,483,263. None of these was applied to overcome the deficiencies pointed out above. It is respectfully submitted that all pending claims are patentable over any combination of these references together with any of the Arai et al., Fujita et al., and/or Comiskey references.

Conclusion

In view of the above, Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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